REMARKS

This is intended as a full and complete response to the Office Action dated March 20, 2007, having a shortened statutory period for response set to expire on June 20, 2007. In view of both the amendments presented above and the following discussion, the Applicants believe all claims are in allowable form.

CLAIM REJECTIONS

Claims 50-51 stand rejected under 35 U.S.C. §102(b) as being unpatentable over *Leverd, et* al., 1999 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, September 8-10, 1999 (hereinafter, "*Leverd*"). Claims 52-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Leverd*, as applied to claim 50, and further in view of *Wolf*, Silicon Processing for VLSI Era; Vol. 1; 1986, Lattice Press, page 432 (hereinafter *"Wolf"*). In response, the Applicants have cancelled claims 50-53 without prejudice to expedite issuance of the application. The Applicants reserve the right to file continuing applications to further prosecute the cancelled subject matter.

ALLOWED CLAIMS

The Applicants thank the Examiner for indicating the allowability of claims 19-49. In light of the cancellation of claims 50-53, the Applicants believe all claims now pending are allowable over the prior art of record.

CONCLUSION

Thus, Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Keith Taboada at (732) 530-9404

so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

May 24, 2007

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